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EXAMINER	
PASIA, REDENTOR M	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,204	WISE ET AL.	
	Examiner	Art Unit	
	REDENTOR M. PASIA	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-11,13-15,17-25,27-29 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11,13-15,17-25,27-29 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on July 8, 2008 has been entered. Claims 1, 9, 13, 17, 23, 27 have been amended. Claims 5, 12, 16, 26, 30 have been canceled. Claim 31 has been added. Claims 1-4, 7-11, 13-15, 17-25, 27-29, and 31 are still pending in this application, with claims 1, 9, 13, 17, 23 and 27 being independent.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 8, 2008 has been entered.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Independent claims 23 and 27 recite the claim limitation, "a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method…" The above-mentioned claim limitation is not shown in the specification.

However, since the above-mentioned claim limitation is included in the original disclosure (original claims), it is suggested by the Examiner to amend the Specification to include **only** the above-mentioned claim limitation. It is important that **no new matter should be included** in amending the Specification in order to avoid possible rejections.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 23-25, 27-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claims 23 and 27 recite the claim limitation, "a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method…" Referring back to the Office Action mailed May 17, 2007, the Examiner has objected to Specification since the Specification does not provide antecedent basis for the above-mentioned claim limitation.

Applicant' Attorney responded to the objection as shown in Applicant's Remarks (received October 17, 2007). Applicant's attorney submits support for the above-mentioned claim limitation and pointed to page 4, lines 7-15 which recite "[S]witch fabric network 100 can include both module-to-module (for example computer systems that support I/O module add-in

slots) and chassis-to-chassis environments (for example interconnecting computers, external storage systems, external Local Area Network (LAN) and Wide Area Network (WAN) access devices in a data-center environment)."

The cited portion of the specification **does not** enable a person skilled in the art to distinguish how a module and/or computer and/or access device relate to a "computer-readable medium".

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1, 5, 7-11, 17, 21-25, 31 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5, 7-9 and 16 of copending Application No. 10/671,203 (hereinafter 203) in view of Martin et al. (US 7,301,898; hereinafter Martin) in further view of Bloch et al. (US 6,922,408; hereinafter Bloch).

As to claim 1, claim 1 of 203 shows the following elements indicated in claim 1 of the instant application.

Instant Application	**Co-pending Application 203**
1. A method, comprising:	1. A method comprising:
providing a link receiver	a link receiver
having a free buffer pool having empty receiver buffers	a free buffer pool at the link receiver; storing the plurality of packets in a plurality of receiver buffers (It is noted that in order to store packets in a receiver, initially, the receiver buffers must be empty.).

providing at the link receiver a plurality of data credits	providing from a link a receiver a plurality of data credits
(data credits) corresponding to the free buffer pool	free buffer pool contains additional data credits (it is noted that the free buffer pool corresponds to data credits (additional or not).).
transmitting the plurality of data credits to a link transmitter;	providing from a link a receiver a plurality of data credits to a link transmitter;
at the link transmitter, assigning at least one of the plurality of data credits to the logical channel;	allocating at the link transmitter the plurality of data credits to a plurality of logical channels;
transmitting a packet from the link transmitter to the link receiver on an ingress link;	transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link;
storing the packet in a plurality of receiver buffers at the link receiver;	storing the plurality of packets in a plurality of receiver buffers at the link receiver;
transmitting a flow control packet from a link receiver to the link transmitter, wherein the flow control packet comprises the additional data credits.	transmitting a flow control packet from a link receiver to the link transmitter, wherein the flow control packet comprises the additional data credits.

Still, ‘203 does not specifically show: at the link transmitter, selecting a logical channel; diminishing the plurality of data credits as the packet is transmitted; transmitting the packet out

of the plurality of receiver buffers at the link receiver on an egress link; placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to the additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use);

diminishing the plurality of data credits as the packet is transmitted (Figure 8, it is noted that in view of Figure 8B, when steady-state is achieved, every frame that is sent out, there is a credit returned for that frame. It is noted that when a credit is returned to the transmitter, the number of credits held in the receiver is decreased (refer to col. 1, line 60 to col. 10, line 20).);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though modified 203 shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, modified 203 does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has

passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claims 5, 7, and 8, claims 5, 7, 8 of further modified 203 shows the following elements indicated in claim 1 of the instant application.

Instant Application	**Further modified Co-pending Application 203**
5. further comprising selecting from the plurality of logical channels to allocated the additional data credits at the link transmitter.	5. further comprising selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter.
7. wherein the link transmitter and the link receiver operate in a switch fabric network.	7. wherein the link transmitter and the link receiver operate in a switch fabric network.
8. wherein the switch fabric network is one of an Infiniband network or SerialIO network.	8. wherein the switch fabric network is one of an Infiniband network or SerialIO network.

As to claim 9, claim 1 of 203 shows the following elements indicated in claim 9 of the instant application.

Instant Application	**Co-pending Application 203**
9. A method, comprising:	1. A method comprising:
at the link transmitter, assigning a data credit to the logical channel;	allocating at the link transmitter the plurality of data credits to a plurality of logical channels;
transmitting a packet from the link transmitter to a link receiver on an ingress link;	transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link;
storing the packet in a plurality of receiver buffers at the link receiver;	storing the plurality of packets in a plurality of receiver buffers at the link receiver;

Still, '203 does not specifically show: at the link transmitter, selecting a logical channel; removing a data credit as the packet is transmitted; transmitting the packet out of the plurality of receiver buffers at the link receiver on an egress link; placing the plurality of receiver buffers into a free buffer pool when the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to the additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use);

removing a data credit as the packet is transmitted (Figure 8, it is noted that in view of Figure 8B, when steady-state is achieved, every frame that is sent out, there is a credit returned

for that frame. It is noted that when a credit is returned to the transmitter, the number of credits held in the receiver is decreased (refer to col. 1, line 60 to col. 10, line 20).);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though modified 203 shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, modified 203 does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that

utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool when the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claim 10, further modified 203 shows that the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty (Martin: Figures 8, shows that in steady-state, for each packet transmitted, there is a credit returned. It is noted that the returned credit also signifies available (claimed empty) buffer space.).

As to claim 11, this claim is rejected using the same reasoning set forth in the rejection of claim 5.

As to claim 17, claim 9 of 203 shows the following elements indicated in claim 17 of the instant application.

Instant Application	**Co-pending Application 203**
17. A switch, comprising:	9. A switch comprising:
a plurality of receiver buffers coupled to receive a packet from a link transmitter,	A plurality of receiver buffers couple to receive packet from a link transmitter
the link transmitter operable to assign a data credit to a logical channel	the link transmitter allocates a plurality of data credits to a plurality of logical channels;
wherein the packet is stored in the plurality of receiver buffers	wherein the packet is stored in the plurality of receiver buffers
a free buffer pool	a free buffer pool
a link receiver flow control algorithm	a link receiver flow control algorithm

Still, 203 does not specifically show: (link transmitter) operable to select a logical channel from a plurality of logical channels; the switch transmits the packet out of the plurality or receiver buffers; (link receiver flow control algorithm) places the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows the link transmitter is operable to select a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels);

the switch transmits the packet out of the plurality of receiver buffers (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.);

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows a flow control algorithm, modified 203 does not specifically show that the link receiver flow control algorithm places the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers (Figure 5 shows a flow chart

that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claims 21 and 22, these claims are rejected using the same reasoning set forth in the rejection of claims 7 and 8, respectively.

As to claim 23, claim 16 of 203 shows the following elements indicated in claim 23 of the instant application.

Instant Application	**Co-pending Application 203**
23. A computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method comprising:	9. A computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method comprising:
at the link transmitter, assigning a data credit to the logical channel;	allocating at the link transmitter the plurality of data credits to a plurality of logical channels;
transmitting a packet from the link transmitter to a link receiver on an ingress link;	transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link;

storing the packet in a plurality of receiver buffers at the link receiver;	storing the plurality of packets in a plurality of receiver buffers at the link receiver;

Still, '203 does not specifically show: at the link transmitter, selecting a logical channel; removing a data credit as the packet is transmitted; transmitting the packet out of the plurality of receiver buffers at the link receiver on an egress link; placing the plurality of receiver buffers into a free buffer pool when the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to the additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use);

removing a data credit as the packet is transmitted (Figure 8, it is noted that in view of Figure 8B, when steady-state is achieved, every frame that is sent out, there is a credit returned for that frame. It is noted that when a credit is returned to the transmitter, the number of credits held in the receiver is decreased (refer to col. 1, line 60 to col. 10, line 20).);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the

system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though modified 203 shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, modified 203 does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool when the packet is transmitting out of the plurality of receiver buffers, wherein the

plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claims 24 and 25, these claims are rejected using the same reasoning set forth in the rejection of claims 10 and 11, respectively.

As to claim 31, modified Martin shows the step of selecting the logical channel from the plurality of logical channels based on traffic conditions of the plurality of logical channels (Martin: col. 9, lines 10-18; The credit allocation or reallocation is carried out by the transmitter dynamically when the credits are returned from the receiving port. Whenever the need of credits for all the VCs in use changes, the transmitter can allocate the returned credits from the receiving port to the VC in need, according to a predetermined formula, such as maximum throughput through the ISL or uniform throughput through each VC in use.).

This is a provisional obviousness-type double patenting rejection.

8. Claims 2-4, 13-15, 18-20, 27-29 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application

No. 10/671,203 (hereinafter 203) in view of Martin et al. (US 7,301,898; hereinafter Martin) in further view of Bloch et al. (US 6,922,408; hereinafter Bloch) in further view of Takase et al. (US 7,023,799; hereinafter Takase).

As to claim 2, further modified 203 shows all of the elements except wherein the ingress link has an ingress link speed, and the egress link has an egress link speed, wherein placing the plurality of receiver buffers into the free buffer pool comprises: if the egress link speed is less than the ingress link speed, placing the plurality of receiver buffers in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed; and if the egress link speed is one of greater than and equal to the ingress link speed, placing the plurality of receiver buffers into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows an ingress link has an ingress link speed, and an egress link has an egress link speed (Figure 11 shows the input line has a rate of 1Gbps, and the output line has a rate of 2.4 Gbps; Similarly, Figure 6 shows different input rates and an output rate of 600 Mbps.), wherein placing the plurality of receiver buffers into the free buffer pool comprises:

if the egress link speed is less than the ingress link speed (Figures 6A, Figure 6C), placing the plurality of receiver buffers in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers (col. 8, lines 1-19; it is noted that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). It is further noted that as long as the level of the leaky bucket repeatedly increases and decreases around the threshold as the lower limit, and the input packets are transferred to the output line without causing excessive residence in the packet buffer.), and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.)

and if the egress link speed is one of greater than and equal to the ingress link speed (Figure 6B, 6D-F), placing the plurality of receiver buffers into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers (col. 8, lines 27-33; packets are continuously transmitted at a rate over the minimum guaranteed bandwidth rate from the packet buffer of the which leaky bucket level is largely below the threshold for a considerable period of time.).

In view of the above, having the system of further modified 203, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of further modified 203 as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum

guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claim 3, further modified 203 shows the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty (Martin: Figures 8, shows that in steady-state, for each packet transmitted, there is a credit returned. It is noted that the returned credit also signifies available (claimed empty) buffer space.).

As to claim 4, further modified Martin shows the portion of the packet is equal to one minus the ratio of the egress link speed to the ingress link speed (Takase: Figure 6C; col. 8, lines 1-18; it is noted that to the leaky bucket, each time a packet is read out from the packet buffer (output queue), "water" of a volume proportional to the packet length is poured. In the case where the packets flow in at a rate over the minimum guaranteed bandwidth of 600Mbps from the input line, if the packet flow out from the packet buffer is controlled at 600 Mbps, the amount of packets residual in the packet queue increases).

As to claim 13, claim 1 of 203 shows the following elements indicated in claim 13 of the instant application.

Instant Application	**Co-pending Application 203**
13. A method, comprising:	1. A method comprising:
at the link transmitter, assigning a data credit to the logical channel;	allocating at the link transmitter the plurality of data credits to a plurality of logical channels;
transmitting a packet from the link transmitter to a link receiver on an ingress link;	transmitting a plurality of packets from the link transmitter to the link receiver on an ingress

	link;
storing the packet in a plurality of receiver buffers at the link receiver;	storing the plurality of packets in a plurality of receiver buffers at the link receiver;

Still, '203 does not specifically show: at the link transmitter, selecting a logical channel; removing a data credit as the packet is transmitted; transmitting the packet out of the plurality of receiver buffers at the link receiver on an egress link; placing the plurality of receiver buffers into a free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed, and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is

noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, modified 203 does not specifically show that the packet is transmitted on an egress link.

Second, even though modified 203 shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, modified 203 does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col.

8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

Still, further modified 203 does not specifically show that the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed.

However, the above-mentioned claim limitation is well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows that the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket,

each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.).

In view of the above, having the system of further modified 203, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of further modified 203 as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claim 14, this claim is rejected using the same reasoning presented in claim 4.

As to claim 15, further modified 203 shows the step of selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter (Martin: Figure 5 shows a plurality of virtual channels; col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.).

As to claim 18, further modified 203 shows all of the elements except the switch is coupled to receive the packet on an ingress link having an ingress link speed, and wherein the switch is coupled to transmit the packet on an egress link having an egress link speed, wherein placing the plurality of receiver buffers into the free buffer pool comprises: if the egress link speed is less than the ingress link speed, the plurality of receiver buffers are placed in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver

buffers, and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed; and if the egress link speed is one of greater than and equal to the ingress link speed, the plurality of receiver buffers are placed into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows a switch is coupled to receive the packet on an ingress link having an ingress link speed, and wherein the switch is coupled to transmit the packet on an egress link having an egress link speed (Figure 11 shows the input line has a rate of 1Gbps, and the output line has a rate of 2.4 Gbps; Similarly, Figure 6 shows different input rates and an output rate of 600 Mbps.), wherein placing the plurality of receiver buffers into the free buffer pool comprises:

if the egress link speed is less than the ingress link speed (Figures 6A, Figure 6C), the plurality of receiver buffers are placed in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers (col. 8, lines 1-19; it is noted that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). It is further noted that as long as the level of the leaky bucket repeatedly increases and decreases around the threshold as the lower limit, and the input packets are transferred to the output line without causing excessive residence in the packet buffer.), and wherein the portion of the packet is

proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.); and

if the egress link speed is one of greater than and equal to the ingress link speed (Figure 6B, 6D-F), the plurality of receiver buffers are placed into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers (col. 8, lines 27-33; packets are continuously transmitted at a rate over the minimum guaranteed bandwidth rate from the packet buffer of the which leaky bucket level is largely below the threshold for a considerable period of time.).

In view of the above, having the system of further modified 203, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of further modified 203 as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claims 19 and 20, these claims are rejected using the same reasoning presented in claims 3 and 4, respectively.

As to claim 27, claim 1 of 203 shows the following elements indicated in claim 27 of the instant application.

Instant Application	**Co-pending Application 203**
at the link transmitter, assigning a data credit to the logical channel;	allocating at the link transmitter the plurality of data credits to a plurality of logical channels;
transmitting a packet from the link transmitter to a link receiver on an ingress link;	transmitting a plurality of packets from the link transmitter to the link receiver on an ingress link;
storing the packet in a plurality of receiver buffers at the link receiver;	storing the plurality of packets in a plurality of receiver buffers at the link receiver;

Still, '203 does not specifically show: a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of early buffer return; at the link transmitter, selecting a logical channel; removing a data credit as the packet is transmitted; transmitting the packet out of the plurality of receiver buffers at the link receiver on an egress link; placing the plurality of receiver buffers into a free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed, and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Martin.

Martin shows a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of early buffer return (col. 10, lines 20-32; the present invention may be implemented in a software format, as a machine readable, machine executable program. The software program executing the present invention can be

loaded into a processor or control module on a switch, or a buffer credit management module on a switch, during a power up initialization or a later set-up. This presumes that the hardware portions of the buffer credit logic are sufficiently programmable or are made sufficiently programmable to handle the changing credit allocations per VC. The present invention may also be implemented in hardware format, as a new switch having the new credit sharing scheme built into the hardware.);

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

In view of the above, having the system of '203, then given the well-established teachings of Martin, it would have been obvious to one of ordinary skill in the art to modify the system of 203 as taught by Martin, in order to maximize the efficiency and throughput across an inter-switch link (ISL) (col. 4, lines 20-21).

First, even though modified 203 shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, modified 203 does not specifically show that the packet is transmitted on an egress link.

Second, even though modified 203 shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, modified 203 does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart

that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of modified 203, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified 203 as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

Still, further modified 203 does not specifically show that the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed.

However, the above-mentioned claim limitation is well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows that the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.).

In view of the above, having the system of further modified 203, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of further modified 203 as taught by Takase in order to provide a traffic

shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claims 28 and 29, these claims are rejected using the same reasoning presented in claims 4 and 5, respectively.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 23-25, 27-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. In this instance, it would be reasonable for a person of ordinary skill in the art to interpret **"computer-readable medium"** as fairly conveying **signals** and **other forms of propagation or transmission media**. The Specification does not provide an explicit and limiting definition of the given terminology, by doing so, the Examiner has given the broadest reasonable interpretation to this claim limitation.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 1, 5, 7-11, 17, 21-25, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (UYS 7,301,898; hereinafter Martin) in view of Bloch et al. (US 6,922,408; hereinafter Bloch).

As to claim 1, Martin shows a method (abstract; a method), comprising:

providing a link receiver (Figures 6-8, receiver 46) having a free buffer pool having empty receiver buffers (col. 5, lines 13-20 shows that each port has a transmitter and a receiver and the available buffer space in the central memory 56 and 58 are allocated among the ports in the switch; col. 1, line 60 to col. 2, line 10; shows that a receiver on a port is allocated a fixed amount of buffer space represented by a fixed number of buffer-to-buffer credits; col. 8, lines 14-28; it is noted that if the receiver advertises the credits to the transmitter, it can also be seen that the presence of the credits shows the presence of free buffer space.),

providing at the link receiver, a plurality of data credits (Figures 6-8, credits are represented as circles) corresponding to the free buffer pool (col. 1, line 60 to col. 2, line 10; col. 8, lines 14-28; shows that a receiver on a port is allocated a fixed amount of buffer space represented by a fixed number of buffer-to-buffer credits.);

transmitting the plurality of credits to a link transmitter (Figures 6-8; credits are transmitted from the receiver to the transmitter);

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assigning at least one of the plurality of data credits to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.);

transmitting a packet from the link transmitter to the link receiver (Figures 6-8, shows transmission of packets (represented by squares) from the transmitter to the receiver) on an ingress link (Figures 6-8; packets are transmitted on an ingress link viewed from the receiver);

diminishing the plurality of data credits as the packet is transmitted (Figure 8, it is noted that in view of Figure 8B, when steady-state is achieved, every frame that is sent out, there is a credit returned for that frame. It is noted that when a credit is returned to the transmitter, the number of credits held in the receiver is decreased (refer to col. 1, line 60 to col. 10, line 20).);

storing the packet in a plurality of receiver buffers at the link receiver (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space).

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

First, even though Martin shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though Martin shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, Martin does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits; and transmitting a flow control packet from a link receiver to the link transmitter, wherein the flow control packet comprises the additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in

Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.); and

transmitting a flow control packet from a link receiver to the link transmitter, wherein the flow control packet comprises the additional data credits (col. 1, lines 43-47 shows a counterexample showing the transmitter is not permitted to send any more data over the VL until it has received a flow control packet from the receiver, indicating that additional credit has become available. It is noted that when additional credits are received (through the reception of a flow control packet), the transmitter can continue to send packets.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claim 5, modified Martin shows the step of selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter (Martin: Figure 5 shows a plurality of virtual channels; col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to

Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.).

As to claim 7, modified Martin shows the link transmitter and the link receiver operate in a switch fabric network (Martin: Figure 1; col. 4, lines 64-67 shows fabric 32 comprises one or more switches; Figures 2-8 shows that each switch contains a transmitter and a receiver).

As to claim 8, modified Martin shows all of the elements except wherein the switch fabric network is one of an Infiniband network and a Serial RapidIO network.

However, the above-mentioned claim limitations are well-established in the art as also evidenced by Bloch. Bloch shows a switch fabric network (Figure 1) that comprises an Infiniband fabric (col. 4, lines 58-63).

In view of the above, having the system of modified Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of modified Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claim 9, Martin shows a method (abstract; a method), comprising:

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assigning a data credit to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.);

transmitting a packet from the link transmitter to a link receiver (Figures 6-8, shows transmission of packets (represented by squares) from the transmitter to the receiver) on an ingress link (Figures 6-8; packets are transmitted on an ingress link viewed from the receiver);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

storing the packet in a plurality of receiver buffers at the link receiver (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

First, even though Martin shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though Martin shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, Martin does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is

transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claim 10, modified Martin shows that the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty (Martin: Figures 8, shows that in steady-state, for each packet transmitted, there is a credit returned. It is noted that the returned credit also signifies available (claimed empty) buffer space.).

As to claim 11, this claim is rejected using the same reasoning set forth in the rejection of claim 5.

As to claim 17, Martin shows a switch (Figure 1-4; shows a switch among a plurality of switches), comprising:

a plurality of receiver buffers coupled to receive a packet from a link transmitter (Figures 1-8; col. 5, lines 13-25 shows the available buffer spaces in the central memory which are allocated to the ports in the switch. Each port has a transmitter and a receiver. It is noted that packets are received by a receiver from the transmitter (as represented by the squares in Figures 6-8).), the link transmitter operable to select a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assign a data credit to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.),

wherein the packet is stored in the plurality of receiver buffers (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space), and

wherein the switch transmits the packet out of the plurality of receiver buffers (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.);

a free buffer pool (col. 5, lines 13-25 shows the available buffer spaces in the central memory which are allocated to the ports in the switch); and

a link receiver flow control algorithm (Figure 6-8; col. 10, lines 19-29 shows that the present invention can be implemented as a software program executing the invention of Martin, can be loaded into a processor or control module on a switch or a buffer credit management module on a switch).

First, even though Martin shows a flow control algorithm, Martin does not specifically show that the link receiver flow control algorithm places the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has

passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claims 21 and 22, these claims are rejected using the same reasoning set forth in the rejection of claims 7 and 8, respectively.

As to claim 23, Martin shows a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of early buffer return (col. 10, lines 20-32; the present invention may be implemented in a software format, as a machine readable, machine executable program. The software program executing the present invention can be loaded into a processor or control module on a switch, or a buffer credit management module on a switch, during a power up initialization or a later set-up. This presumes that the hardware portions of the buffer credit logic are sufficiently programmable or are made sufficiently programmable to handle the changing credit allocations per VC. The present invention may also be implemented in hardware format, as a new switch having the new credit sharing scheme built into the hardware.) the instructions comprising:

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assigning a data credit to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that

when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.);

transmitting a packet from the link transmitter to a link receiver (Figures 6-8, shows transmission of packets (represented by squares) from the transmitter to the receiver) on an ingress link (Figures 6-8; packets are transmitted on an ingress link viewed from the receiver);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

storing the packet in a plurality of receiver buffers at the link receiver (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

First, even though Martin shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though Martin shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, Martin does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

As to claims 24 and 25, these claims are rejected using the same reasoning set forth in the rejection of claims 10 and 11, respectively.

As to claim 31, modified Martin shows the step of selecting the logical channel from the plurality of logical channels based on traffic conditions of the plurality of logical channels (Martin: col. 9, lines 10-18; The credit allocation or reallocation is carried out by the transmitter dynamically when the credits are returned from the receiving port. Whenever the need of credits for all the VCs in use changes, the transmitter can allocate the returned credits from the receiving port to the VC in need, according to a predetermined formula, such as maximum throughput through the ISL or uniform throughput through each VC in use.).

15. Claims 2-4, 13-15, 18-20, 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (UYS 7,301,898; hereinafter Martin) in view of Bloch et al. (US 6,922,408; hereinafter Bloch) in further view of Takase et al. (US 7,023,799; hereinafter Takase).

As to claim 2, modified Martin shows all of the elements except wherein the ingress link has an ingress link speed, and the egress link has an egress link speed, wherein placing the plurality of receiver buffers into the free buffer pool comprises:

if the egress link speed is less than the ingress link speed, placing the plurality of receiver buffers

in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed; and if the egress link speed is one of greater than and equal to the ingress link speed, placing the plurality of receiver buffers into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows an ingress link has an ingress link speed, and an egress link has an egress link speed (Figure 11 shows the input line has a rate of 1Gbps, and the output line has a rate of 2.4 Gbps; Similarly, Figure 6 shows different input rates and an output rate of 600 Mbps.), wherein placing the plurality of receiver buffers into the free buffer pool comprises:

if the egress link speed is less than the ingress link speed (Figures 6A, Figure 6C), placing the plurality of receiver buffers in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers (col. 8, lines 1-19; it is noted that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). It is further noted that as long as the level of the leaky bucket repeatedly increases and decreases around the threshold as the lower limit, and the input packets are transferred to the output line without causing excessive residence in the packet buffer.), and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is

noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.)

and if the egress link speed is one of greater than and equal to the ingress link speed (Figure 6B, 6D-F), placing the plurality of receiver buffers into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers (col. 8, lines 27-33; packets are continuously transmitted at a rate over the minimum guaranteed bandwidth rate from the packet buffer of the which leaky bucket level is largely below the threshold for a considerable period of time.).

In view of the above, having the system of modified Martin, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of modified Martin as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claim 3, further modified Martin shows the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty (Martin: Figures 8, shows that in steady-state, for each packet transmitted, there is a credit returned. It is noted that the returned credit also signifies available (claimed empty) buffer space.).

As to claim 4, further modified Martin shows the portion of the packet is equal to one minus the ratio of the egress link speed to the ingress link speed (Takase: Figure 6C; col. 8, lines 1-18; it is noted that to the leaky bucket, each time a packet is read out from the packet buffer

(output queue), "water" of a volume proportional to the packet length is poured. In the case where the packets flow in at a rate over the minimum guaranteed bandwidth of 600Mbps from the input line, if the packet flow out from the packet buffer is controlled at 600 Mbps, the amount of packets residual in the packet queue increases).

As to claim 13, Martin shows a method (abstract; a method), comprising:

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assigning a data credit to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.);

transmitting a packet from the link transmitter to a link receiver (Figures 6-8, shows transmission of packets (represented by squares) from the transmitter to the receiver) on an ingress link (Figures 6-8; packets are transmitted on an ingress link viewed from the receiver);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

storing the packet in a plurality of receiver buffers at the link receiver (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

First, even though Martin shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though Martin shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, Martin does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

Still, modified Martin does not specifically show that the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed.

However, the above-mentioned claim limitation is well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows that the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.).

In view of the above, having the system of modified Martin, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of modified Martin as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claim 14, this claim is rejected using the same reasoning presented in claim 4.

As to claim 15, further modified Martin shows the step of selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter (Martin: Figure 5 shows a plurality of virtual channels; col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.).

As to claim 18, modified Martin shows all of the elements except the switch is coupled to receive the packet on an ingress link having an ingress link speed, and wherein the switch is coupled to transmit the packet on an egress link having an egress link speed, wherein placing the plurality of receiver buffers into the free buffer pool comprises: if the egress link speed is less

than the ingress link speed, the plurality of receiver buffers are placed in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed; and if the egress link speed is one of greater than and equal to the ingress link speed, the plurality of receiver buffers are placed into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows a switch is coupled to receive the packet on an ingress link having an ingress link speed, and wherein the switch is coupled to transmit the packet on an egress link having an egress link speed (Figure 11 shows the input line has a rate of 1Gbps, and the output line has a rate of 2.4 Gbps; Similarly, Figure 6 shows different input rates and an output rate of 600 Mbps.), wherein placing the plurality of receiver buffers into the free buffer pool comprises:

if the egress link speed is less than the ingress link speed (Figures 6A, Figure 6C), the plurality of receiver buffers are placed in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers (col. 8, lines 1-19; it is noted that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). It is further noted that as long as the level of the leaky bucket repeatedly increases and decreases around the

threshold as the lower limit, and the input packets are transferred to the output line without causing excessive residence in the packet buffer.), and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.); and

if the egress link speed is one of greater than and equal to the ingress link speed (Figure 6B, 6D-F), the plurality of receiver buffers are placed into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers (col. 8, lines 27-33; packets are continuously transmitted at a rate over the minimum guaranteed bandwidth rate from the packet buffer of the which leaky bucket level is largely below the threshold for a considerable period of time.).

In view of the above, having the system of modified Martin, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of modified Martin as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claims 19 and 20, these claims are rejected using the same reasoning presented in claims 3 and 4, respectively.

As to claim 27, Martin shows a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of early buffer return

(col. 10, lines 20-32; the present invention may be implemented in a software format, as a machine readable, machine executable program. The software program executing the present invention can be loaded into a processor or control module on a switch, or a buffer credit management module on a switch, during a power up initialization or a later set-up. This presumes that the hardware portions of the buffer credit logic are sufficiently programmable or are made sufficiently programmable to handle the changing credit allocations per VC. The present invention may also be implemented in hardware format, as a new switch having the new credit sharing scheme built into the hardware.), the instructions comprising:

at the link transmitter, selecting a logical channel (Figure 7, virtual channel VC4 is in use; Figure 8, VC2 and VC4 are in use) from a plurality of logical channels (Figure 5 shows a plurality of virtual channels) and assigning a data credit to the logical channel (col. 8, line 35 to col. 9, line 18; the transmitter controls the allocation of the credits to each VC. It is noted that when 1 frame carrying VC (i.e. VC4 as to Figure 7) is in use, the transmitter allocates (1,1,1,1,21,1,1,1). Similar situation applies to Figure 8 example.);

transmitting a packet from the link transmitter to a link receiver (Figures 6-8, shows transmission of packets (represented by squares) from the transmitter to the receiver) on an ingress link (Figures 6-8; packets are transmitted on an ingress link viewed from the receiver);

removing a data credit at the link transmitter as the packet is transmitted (Figure 8, col. 1, line 60 to col. 10, line 20; the transmitters initialize their credit counters to the number of credits advertised by the receivers. Both the transmitter and receivers keep track of the use of the buffer space using the number of credits and credit counters. It is noted that each time a frame is

transmitted, the transmitting port keeps track of this by reducing its transmitter credit counter, which indicates how many more frames can be sent.);

storing the packet in a plurality of receiver buffers at the link receiver (col. 1, line 60 to col. 2, line 10; a receiver on a port is allocated a fixed amount of buffer space to store received frames; each time a frame is received by the receiver, the frame is stored in a buffer space);

transmitting the packet out of the plurality of receiver buffers at the link receiver (col. 2, lines 1-20; shows that the frame is retransmitted by a transmitter on the receiving switch; it is noted that since the frame was initially received then stored in the buffers, the frame that was retransmitted was retransmitted out of the buffers.).

First, even though Martin shows the step of transmitting the packet out of the plurality of receiver buffers at the link receiver, as discussed above, Martin does not specifically show that the packet is transmitted on an egress link.

Second, even though Martin shows that given a steady-state condition as shown in Figure 8, every packet sent out, there is credit returned, however, Martin does not specifically show the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed and wherein the plurality of receiver buffers correspond to additional data credits.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Bloch. Bloch shows a method of link-level flow control that includes establishing a plurality of logical links between a transmitting entity and a receiving entity in a network that

utilizes credit allocation wherein the transmission of data over a given logical link is responsive to the allocation of credits (abstract).

First, Bloch specifically shows the packet is transmitted on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission. Col. 8, lines 13-21; Figure 1, 5; shows the method performed in relation to the network shown in Figure 1, where it is noted that the method is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward/outward/egress transmission toward the network.).

Second, Bloch shows the step of placing the plurality of receiver buffers into the free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the plurality of receiver buffers correspond to additional data credits (Figure 5 shows a flow chart that illustrates a method of re-allocation of credits in the receive queue 28 after a data packet has passed out of buffer 25; col. 8, lines 22-51 shows the different scenarios of re-allocation of credits (or buffer spaces) when the packet was passed out of the buffer; col. 3, lines 28-53.).

In view of the above, having the system of Martin, then given the well-established teaching of Bloch, it would have been obvious to one of ordinary skill in the art to modify the system of Martin as taught by Bloch in order to enhance the efficiency of buffer memory use in switching devices in a packet switching fabric (col. 2, lines 2-3).

Still, modified Martin does not specifically show that the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed.

However, the above-mentioned claim limitation is well-established in the art as evidenced by Takase. Takase related to a traffic shaper and a bandwidth controller for a variable-length packet, for transmitting a received packet temporarily stored in a buffer memory

to an output circuit in conformity with a minimum guaranteed bandwidth preliminarily designated, by a bandwidth control using a leaky bucket (col. 1, lines 7-14).

Specifically, Takase shows that the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; it is noted that, to the leaky bucket, each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input rate and the output rate.).

In view of the above, having the system of modified Martin, then given the well-established teaching of Takase, it would have been obvious to one of ordinary skill in the art to modify the system of modified Martin as taught by Takase in order to provide a traffic shaper capable of transferring variable-length packets while guaranteeing the minimum guaranteed bandwidth to each traffic and effectively using an unoccupied bandwidth of a communication line (col. 2, lines 58-62).

As to claims 28 and 29, these claims are rejected using the same reasoning presented in claims 4 and 5, respectively.

Response to Arguments

16. Applicant's arguments with respect to claims 1-4, 7-11, 13-15, 17-25, 27-29, and 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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